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ATTORNEY DOCKET NO.: S. CHITTIPEDDI 79 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Sailesh Chittipeddi

Serial No.: 09/596,382

Filed: June 16, 2000

For: A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR

Group: 2812

Examiner: H. Jey Tsai

Commissioner for Patents
Washington, D. C. 20231

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this correspondence, including the attachments listed, is being deposited as First Class Mail with the United States Postal Service, in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the date shown below.

April 15, 2003 Stephanie Pruitt
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ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated November 6, 2002, of Claims 1-2, 6-8 and 10-12. The Appellant submits this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $ 320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorizes the Commissioner

to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

A currently pending appeal regarding application number 09/595,642, filed June 16, 2000, assignee, Agere Systems, Inc., will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

The Appellant originally submitted Claims 1-22 in the application. Pursuant to an election, the Appellant elected to pursue Claims 1-12 and canceled Claims 13-22 without prejudice or disclaimer. Subsequent to the election, the Appellant also canceled Claims 3-5 and 9 without prejudice or disclaimer. Therefore, Claims 1-2, 6-8 and 10-12 are pending and currently stand rejected with no claims objected to or allowed. Claims 1-2, 6-8 and 10-12 are being appealed.

IV. STATUS OF THE AMENDMENTS

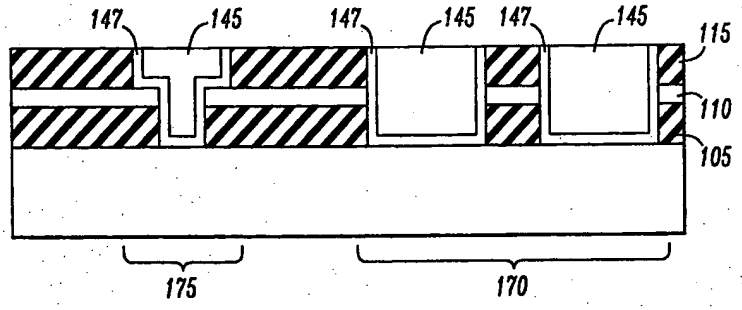
On July 29, 2002, the Appellant filed an amendment to Claims 1, 2, 6, 7 and 10 and canceled Claims 3-5 and 9 without disclaimer or prejudice. By an office action dated November 6, 2002, the Examiner notified the Appellant that the amendment had been received and entered and issued a final rejection. After response by Appellant, the Examiner issued an advisory action dated January 28, 2003. On March 4, 2003, the Appellant filed a Notice of Appeal.

V. SUMMARY OF THE INVENTION

Among other things, the present invention provides for a method of manufacturing an integrated circuit with capacitors and dual damascene structures in a single level of metallization.

As shown in the illustration below, which is FIG. 7 in the present application, the device includes a dual damascene structure 175 located adjacent capacitor structures 170. The dual damascene structure 175 is formed in an interlevel layer 105 and includes at least a groove and a via where the via extends through a stop layer 110. The capacitor structures 170 have a first electrode and a second electrode formed through the layer 105 wherein the first and second electrodes are each defined by openings 145 that extend through the stop layer 110 and the interlevel layer 105.

FIG. 7



VI. ISSUES

Whether Claims 1, 2, 6-8 and 10-12 are unpatentable under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6,228,711 to Hsieh (Hseih) in view of U.S. Patent No. 6,207,560 to Lee (Lee).

VII. GROUPING OF THE CLAIMS

Claims 1, 2, 6-8 and 10-12 stand or fall together

VIII. SUMMARY OF THE REFERENCE RELIED ON BY THE EXAMINER

A. Hsieh. Hsieh describes a method of fabricating a dynamic random access memory with a node contact opening and a capacitor combined in a single damascene opening 346. As shown below in FIG's 3J of Hsieh, separate but identical capacitors are formed in two damascene openings 346. Each of the capacitors has a first electrode 348a defined by a damascene opening 346. Located within the opening 346 is a dielectric layer 356 defined by a hemispherical -grained silicon layer 350a that is deposited over the first electrode 348a to increase the effective capacitor plate area. Deposited in the same opening 346 and defined by the dielectric layer 356 is the second capacitor electrode 358.

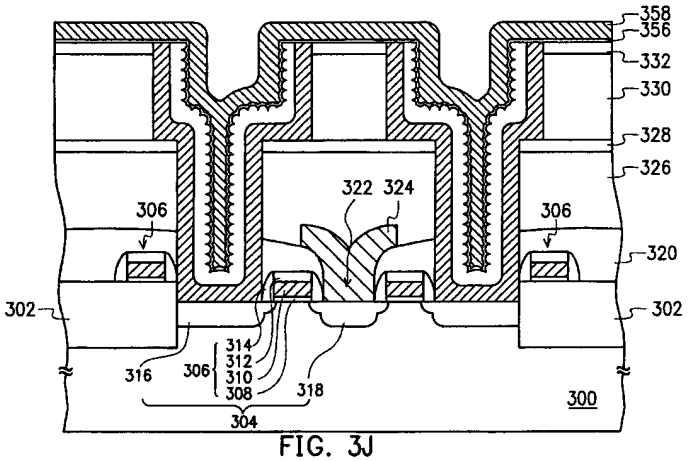


FIG. 3J

B. Lee. Lee describes a dual damascene method for manufacturing a multilevel metal interconnect within a thin film resistor 204a. Lee is chiefly directed towards maintaining resistance values while decreasing resistor dimensions. The relevant embodiment in Lee is shown in FIG 2D illustrated below. Shown are trenches 214, 216 and 218 and a via hole 224. The trenches are formed in an insulating layer 202 and only partially extend into such layer 202, and a thin film resistor 204a contacts the trenches 214 and 216.

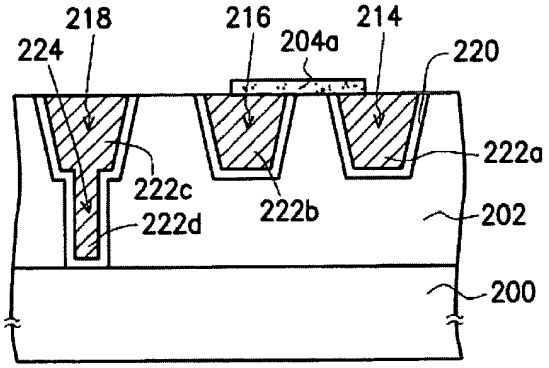


FIG. 2D

IX. THE APPELLANT'S ARGUMENTS

The Appellant respectfully disagrees with the Examiner's conclusion that the claimed inventions are obvious over Hsieh in view of Lee. The Examiner relies chiefly on Hsieh for teaching or suggesting the capacitors recited in the presently claimed inventions and relies on Lee for the teaching of a dual damascene structure 218. Initially, the Appellant wishes to point out that the combination of Hsieh and Lee does not teach or suggest forming at least two openings 145 in a layer 105 for "a" capacitor 170 where each of the electrodes are defined by an opening that extends

through the stop layer and the layer. To the contrary, the combination teaches or suggests forming two openings 346 in a layer for "two" capacitors, such as that disclosed in Hsieh. These two openings consist of a damascene type of structure wherein each of the electrodes in each capacitor is deposited in two different openings. Lee simply teaches a damascene structure adjacent a thin film resistor. Thus, the combined teachings differs significantly from the present invention.

The Appellant's invention recites a first electrode and second electrode, where each is defined by an opening 145 extending through the layer and stop layer. Contrast this with the combined teachings or suggestions in Hsieh where the capacitor electrodes 348a and 358 are defined by two different openings 346 in the layer, only one of which extends through the stop layer. The first opening terminates at the stop layer and the second opening extends through the stop layer and down to the source/drain regions adjacent the gates 306. It is important to note that both electrodes of each capacitor extends through each of the two openings that define each of the two capacitors shown and described in Hsieh. Thus, Hsieh is directed to a method of forming a capacitor where only one of the two openings, in which the two electrodes are deposited, extends through the stop layer. Moreover, Hsieh provides no suggestion or motivation to form such a structure as recited in the claimed inventions without the improper use of hindsight because doing so would decrease capacitance values and increase the capacitor spacing/size requirements, complexity and costs, in direct contrast to the objectives specified by Hsieh. (Column 3, lines 15-33).

Lee when combined with Hsieh does not cure the deficient teachings of Hsieh. While the structure in Lee is a dual damascene structure, it teaches nothing more that would be sufficient to cure the deficient teachings of Hsieh, because it also fails to teach or suggest a second capacitor electrode defined by an opening that extends through a layer and stop layer. Lee does not disclose

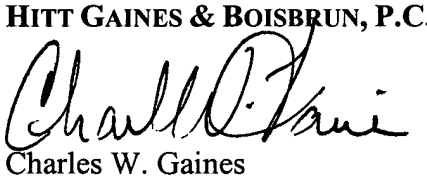
an insulating layer 202 that includes a stop layer, nor does it describe openings (trenches 214 and 216) that extend through the insulating layer 202 to a stop layer. Thus, Lee adds nothing to Hsieh. Moreover, the trenches 216 and 214 are not capacitors, but instead contacts for the thin film resistor. Because Lee is directed towards maintaining resistance values while decreasing resistor dimensions, Lee does not address or suggest capacitor electrodes defined by openings extending through a layer and stop layer. (Column 1, lines 46-57). Therefore, the combination does not teach or suggest each and every element of the presently claimed inventions.

In conclusion, the combination of Hsieh and Lee, fails to teach or suggest the invention recited in independent Claims 1 and 10, and therefore, the combination fails to establish a *prima facie* case of obviousness with respect to the claimed invention.

Because Claims 2 and 6-8 are dependent upon Claim 1 and Claims 11 and 12 are dependent on Claim 10, the combination also fails to establish a *prima facie* case of obviousness with respect to these claims. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of the Appellant's pending claims.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



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X. APPENDIX A - CLAIMS

1. (Amended) A method for manufacturing an integrated circuit comprising:

forming a layer having a stop layer;

forming an opening for a dual damascene structure in the layer that includes at least a groove and a via where the via extends through the stop layer; and

forming at least two openings in the layer for a capacitor having a first electrode and a second electrode, wherein the first and second electrodes are each defined by an opening that extends through the stop layer and the layer.

2. (Amended) The method of claim 1 wherein forming an opening for a dual damascene structure and forming at least two openings in the layer for a capacitor occur at substantially the same time.

6. (Amended) The method of claim 1 further comprising:

filling the opening for a dual damascene structure with a conductive material; and

filling the at least two openings in the layer for a capacitor with a conductive material.

7. (Amended) The method of claim 6 wherein filling the opening for a dual damascene structure and filling the at least two openings in the layer for a capacitor occur at substantially the same time.

8. The method of claim 1 wherein the layer comprises a plurality of layers.

10. (Amended) A method of manufacturing an integrated circuit comprising:

forming a plurality of layers;

partially forming a dual damascene structure by forming a first opening in a least one of the plurality of layers; and

partially forming a capacitor by forming second and third openings in the at least one of the plurality of layers, wherein the second and third openings extend through the at least one of the plurality of layers.

11. The method of claim 10 wherein the first, second, and third openings have substantially the same width.

12. The method of claim 10 wherein the second and third openings have a first width and the first opening has a second width different from the first width.